查询GS9025A供应商

GENNUM CORPORATION

GENLINX™ II GS9025A
Serial Digital Receiver

PRELIMINARY DATA SHEET

FEATURES

- **SMPTE 259M compliant**
- **operational to 540Mb/s**
- **automatic cable equalization (typically greater than 350m of high quality cable at 270Mb/s)**
- **adjustment-free operation**
- **auto-rate selection (5 rates) with manual override**
- **single external VCO resistor for operation with five input data rates**
- **data rate indication output**
- **serial data outputs muted and serial clock remains active when input data is lost**
- **operation independent of SAV/EAV sync signals**
- **signal strength indicator output**
- **carrier detect with programmable threshold level**
- **power savings mode (output serial clock disable)**

APPLICATIONS

Cable equalization plus clock and data recovery for all high speed serial digital interface applications involving SMPTE 259M and other data standards.

DESCRIPTION

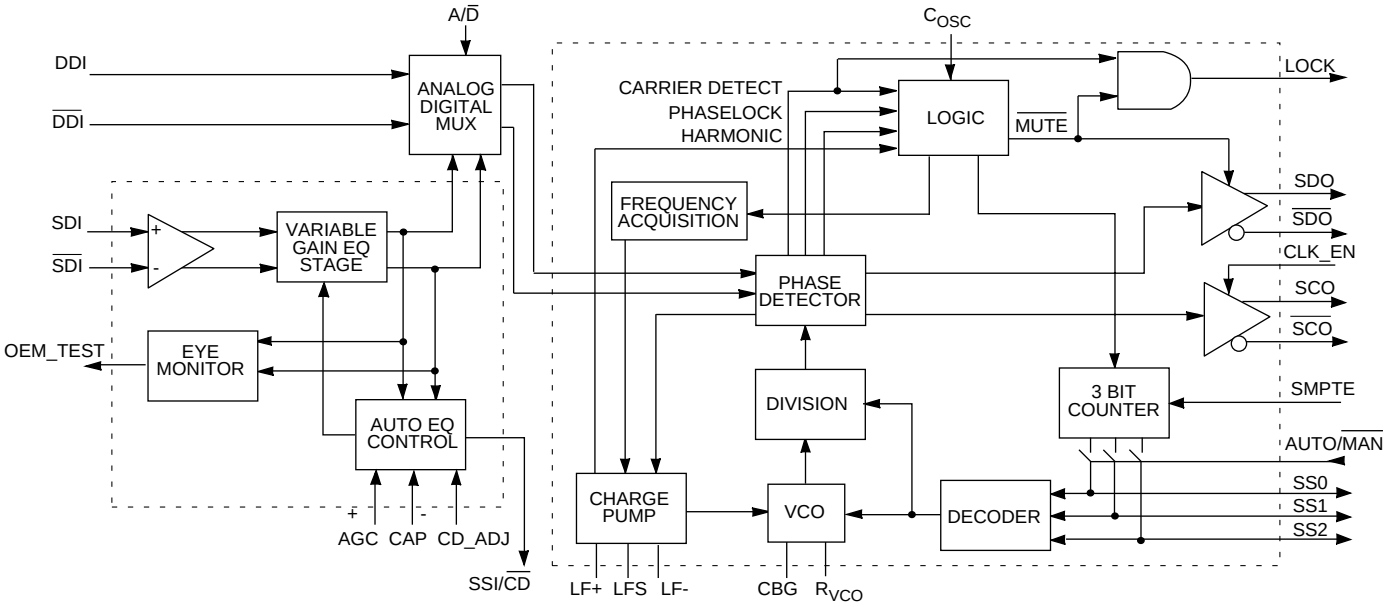
The GS9025A provides automatic cable equalization and high performance clock and data recovery for serial digital signals. The GS9025A receives either single-ended or differential serial digital data and outputs differential clock and retimed data signals at PECL levels (800mV). The on-board cable equalizer provides up to 40dB of gain at 200MHz which typically results in equalization of greater than 350m of high quality cable at 270Mb/s.

The GS9025A operates in either auto or manual data rate selection mode. In both modes, the GS9025A requires only one external resistor to set the VCO centre frequency and provides adjustment free operation.

The GS9025A has dedicated pins to indicate signal strength/carrier detect, LOCK and data rate. Optional external resistors allow the carrier detect threshold level to be customized to the user's requirement. In addition, the GS9025A provides an 'Output Eye Monitor Test' (OEM_TEST) for diagnostic testing of signal integrity after equalization, prior to reslicing. The serial clock outputs can also be disabled to reduce power. The GS9025A operates from a single +5 or -5 volt supply.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS9025ACQM	44 pin MQFP Tray	0°C to 70°C
GS9025ACTM	44 pin MQFP Tape	0°C to 70°C



BLOCK DIAGRAM

GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
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ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage (V_S)	5.5V
Input Voltage Range (any input)	V_{CC} + 0.5 to V_{EE} - 0.5V
Operating Temperature Range	0°C ≤ T_A ≤ 70°C
Storage Temperature Range	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec)	260°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, T_A = 25°C unless otherwise stated, R_{LF} = 1.8k, C_{LF1} = 15nF, C_{LF2} = 3.3pF

PARAMETER	CONDITION	MIN	TYPICAL[1]	MAX	UNITS	NOTES	TEST LEVEL
Supply Voltage		4.75	5	5.25	V		1
Supply Current	CLK_EN = 0	-	115		mA		1
	CLK_EN = 1	-	125				
SDI Common Mode Voltage		-	2.5	-	V		1
DDI Common Mode Input Voltage Range		V_{EE}+(V_{DIFF}/2)	0.4 to 4.6	V_{CC}-(V_{DIFF}/2)	V	2	1
DDI Differential Input Drive		200	800	2000	mV		1
SSI/$\overline{CD}$ Output Current	Source, C_{LMAX} = 50pF, R_L = open cct.	-	-	18	µA		3
	Source, C_{LMAX} = 50pF, R_L=5K	-	-	110	µA		3
	Sink	-	1.0	1.5	mA		3
AGC Common Mode Voltage		-	2.7	-	V		1
OEM_TEST Bias Potential		-	4.5	-	V	5	1
A/$\overline{D}$, AUTO/MAN, SMPTE, SS[2:0] Input Voltage	High	2.0	-	-	V		1
	Low	-	-	0.8			
CLK_EN Input Voltage	High	2.5	-	-	V		1
	Low	-	-	0.8			
LOCK Output Sink Current		500	-	-	µA	3	1
SS[2:0] Output Voltage	High	4.4	4.7	-	V		1
	Low	-	0.2	0.4			
SS[2:0] Source Current	Auto Mode	180	300	-	µA		1
SS[2:0] Sink Current	Auto Mode	0.6	1.0	-	mA		
SS[2:0] Source Current	Manual Mode	-	0	-	µA	4	1

DC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 5.0V, T_A = 25°C unless otherwise stated, R_{LF} = 1.8k, C_{LF1} = 15nF, C_{LF2} = 3.3pF

PARAMETER	CONDITION	MIN	TYPICAL[1]	MAX	UNITS	NOTES	TEST LEVEL
SS[2:0] Sink Current	Manual Mode	-	0.8	5	µA		
CLK_EN Source Current	Low	-	26	55	µA		1

NOTES

1. TYPICAL - measured on EB9025A board.
2. V_{DIFF} is the differential input signal swing.
3. LOCK is an open collector output and requires an external pullup resistor.
4. Pins SS[2:0] are outputs in AUTO mode and inputs in MANUAL mode.
5. If OEM_TEST is permanently enabled, operating temperature range is limited from 0°C to 60°C inclusive.

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, V_{EE} = 0V, T_A = 25°C unless otherwise stated, R_{LF} = 1.8k, C_{LF1} = 15nF, C_{LF2} = 3.3pF

PARAMETER	CONDITIONS	MIN	TYPICAL[1]	MAX	UNITS	NOTES	TEST LEVEL
Serial Data Rate	SDI	143	-	540	Mb/s		1
Maximum Equalizer Gain	@ 200MHz	-	40	-	dB		7
Additive Jitter [Pseudorandom (2^{23} -1)]	270Mb/s, 300m (Belden 8281)	-	300	-	ps p-p	2, 8	3
	540Mb/s, 100m (Belden 8281)	-	275	-			
Intrinsic Jitter [Pseudorandom (2^{23} -1)]	270Mb/s	-	185	see Figure 12	ps p-p	2, 7	4
	540Mb/s	-	164				
Intrinsic Jitter [Pathological (SDI checkfield)]	270Mb/s	-	462	see Figure 13	ps p-p	2, 7	1
	360Mb/s	-	308				
	540Mb/s	-	260				
Input Jitter Tolerance	270Mb/s	0.40	0.56	-	UI p-p	3, 7	1
	540Mb/s	0.35	0.43	-			
Lock Time - Synchronous Switch	t_{switch} < 0.5µs, 270Mb/s	-	1	-	µs	4	7
	0.5µs< t_{switch} <10ms	-	1	-	ms		
	t_{switch} > 10 ms	-	4	-	ms		
Lock Time - Asynchronous Switch	Loop Bandwidth = 6MHz @ 540Mb/s	-	10	-	ms	5	7
Carrier Loss Time		0.5	1	2	µs	6	7
SDO to SCO Synchronization		-200	0	200	ps		7

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, V_{EE} = 0V, T_A = 25°C unless otherwise stated, R_{LF} = 1.8k, C_{LF1} = 15nF, C_{LF2} = 3.3pF

PARAMETER	CONDITIONS	MIN	TYPICAL[1]	MAX	UNITS	NOTES	TEST LEVEL
SDO, SCO Output Signal Swing	75Ω DC load	600	800	1000	mV p-p		1
SDO, SCO Rise & Fall times	20%-80%	200	300	400	ps		7
SDI/$\overline{\text{SDI}}$ Input Resistance		-	10	-	kΩ	8	6
SDI/$\overline{\text{SDI}}$ Input Capacitance		-	1.0	-	pF	8	6
SDI/$\overline{\text{SDI}}$ Input Return Loss	at 270MHz	15	20	-	dB	8	6
Carrier Detect Response Time	Carrier Applied, C_L<50pF, R_L=open cct.	-	3	-	µs	8	6
	Carrier Removed, C_L<50pF, R_L=open cct.	-	30	-			

NOTES

1. TYPICAL - measured on EB9025A board.
2. Characterized 6 sigma rms.
3. IJT measured with sinusoidal modulation beyond Loop Bandwidth (at 6.5MHz).
4. Synchronous switching refers to switching the input data from one source to another source which is at the same data rate (ie. line 10 switching for component NTSC).
5. Asynchronous switching refers to switching the input data from one source to another source which is at a different data rate.
6. Carrier Loss Time refers to the response of the SDO output from valid re-clocked input data to mute mode when the input signal is removed.
7. Using the DDI input, A/$\overline{\text{D}}$=0.
8. Using the SDI input, A/$\overline{\text{D}}$=1.

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.

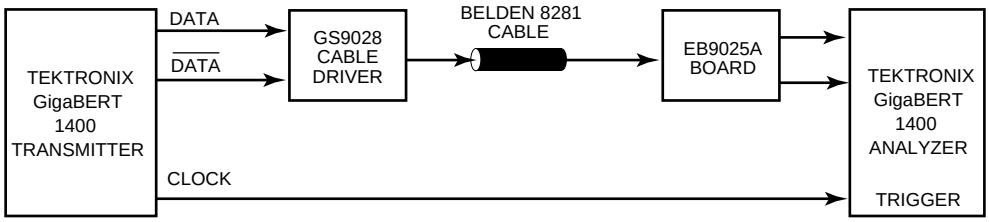
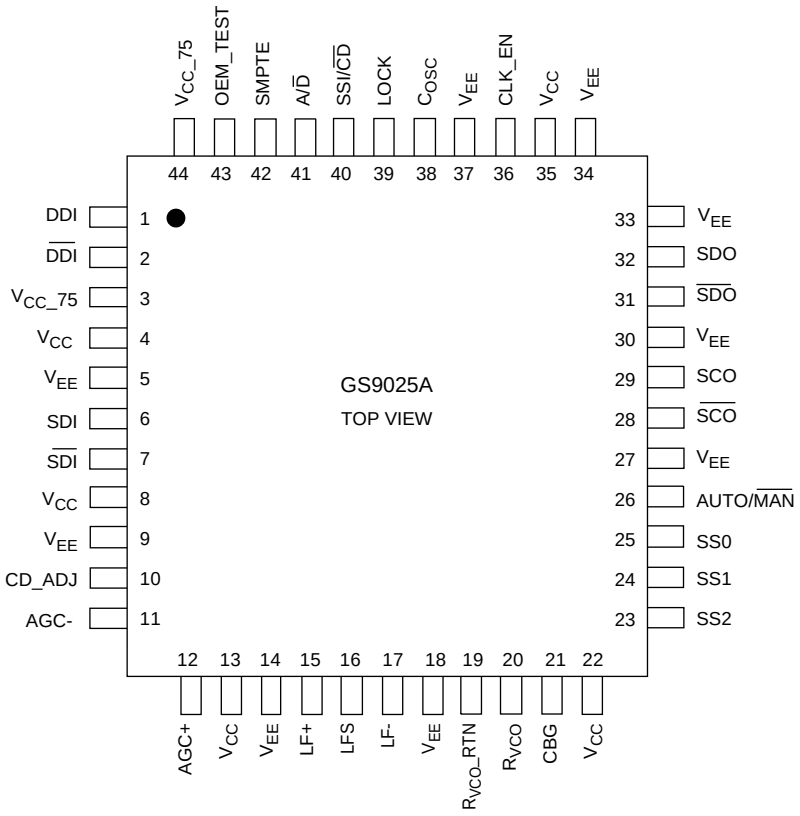


Fig. 1 Test Setup for Figures 6 - 13

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1, 2	DDI/$\overline{\text{DDI}}$	I	Digital data inputs (Differential ECL/PECL).
3, 44	V_{CC}_75	I	Power supply connection for internal 75Ω pullup resistors connected to DDI/$\overline{\text{DDI}}$.
4, 8, 13, 22, 35	V_{CC}	I	Most positive power supply connection.
5, 9, 14, 18, 27, 30, 33, 34, 37	V_{EE}	I	Most negative power supply connection.
6, 7	SDI/$\overline{\text{SDI}}$	I	Differential analog data inputs.
10	CD_ADJ	I	Carrier detect threshold adjust.
11, 12	AGC-, AGC+	I	External AGC capacitor.
15	LF+	I	Loop filter component connection.
16	LFS	I	Loop filter component connection.
17	LF-	I	Loop filter component connection.
19	R_{VCO}_RTN	I	Frequency setting resistor return connection.
20	R_{VCO}	I	Frequency setting resistor connection.
21	CBG	I	Internal bandgap voltage filter capacitor.
23, 24, 25	SS[2:0]	I/O	Data rate indication (auto mode) or data rate select (manual mode). TTL/CMOS compatible I/O. In auto mode, these pins can be left unconnected.
26	AUTO/$\overline{\text{MAN}}$	I	Auto or manual mode select. TTL/CMOS compatible input.

PIN DESCRIPTIONS (continued)

NUMBER	SYMBOL	TYPE	DESCRIPTION
28, 29	SCO/$\overline{\text{SCO}}$	O	Serial clock output. SCO/$\overline{\text{SCO}}$ are differential current mode outputs and require external 75Ω pullup resistors.
31, 32	SDO/$\overline{\text{SDO}}$	O	Equalized and reclocked serial digital data outputs. SDO/$\overline{\text{SDO}}$ are differential current mode outputs and require external 75Ω pullup resistors.
36	CLK_EN	I	Clock enable. When HIGH, the serial clock outputs are enabled.
38	COSC	I	Timing control capacitor for internal system clock.
39	LOCK	O	Lock indication. When HIGH, the GS9025A is locked. LOCK is an open collector output and requires an external 10kΩ pullup resistor.
40	SSI/$\overline{\text{CD}}$	O	Signal strength indicator/Carrier detect.
41	A/$\overline{\text{D}}$	I	Analog/Digital select.
42	SMPTE	I	SMPTE/Other data rate select. TTL/CMOS compatible input.
43	OEM_TEST	O	Output 'Eye' monitor test. Single-ended current mode output that requires an external 50Ω pullup resistor. This feature is recommended for debugging purposes only. If enabled during normal operation, the maximum operating temperature is rated to 60°C.

TYPICAL PERFORMANCE CURVES (V_S = 5V, T_A = 25°C unless otherwise shown)

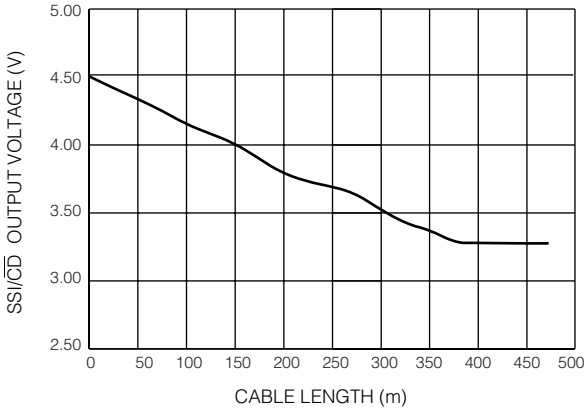


Fig. 2 SSI/$\overline{CD}$ Voltage vs. Cable Length (Belden 8281) (CD_ADJ = 0V)

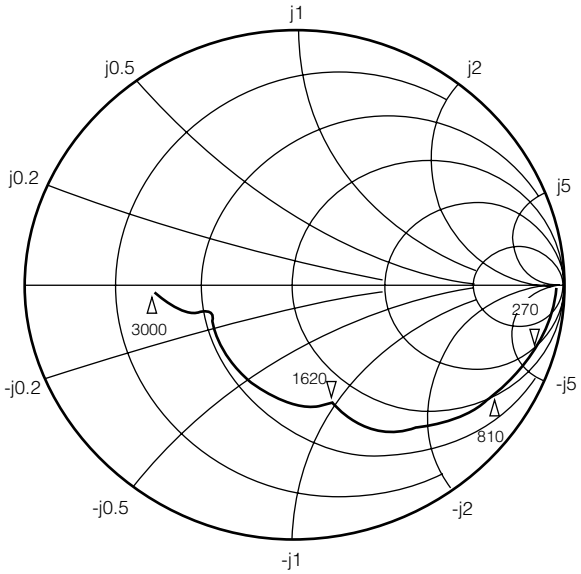


Fig. 5 Input Impedance

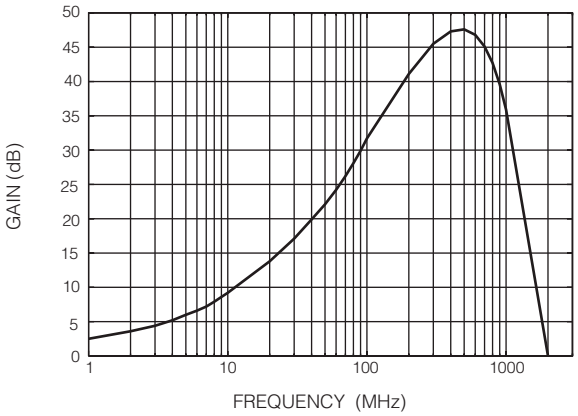


Fig. 3 Equalizer Gain vs. Frequency

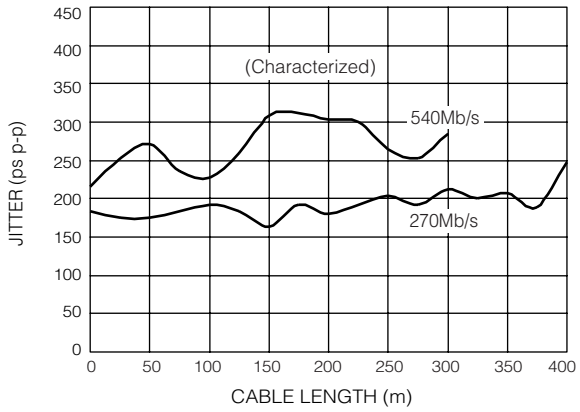


Fig. 6 Typical Additive Jitter vs. Input Cable Length (Belden 8281) Pseudorandom (2^{23}-1)

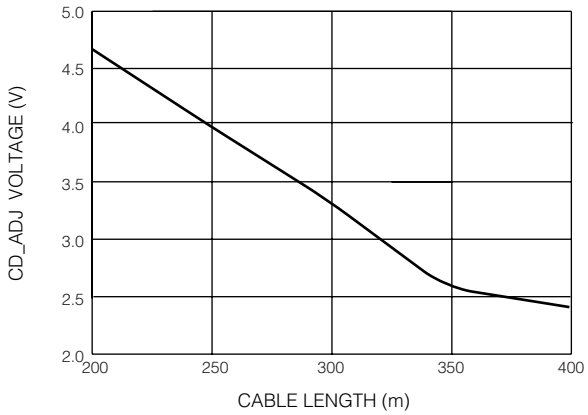


Fig. 4 Carrier Detect Adjust Voltage Threshold Characteristics

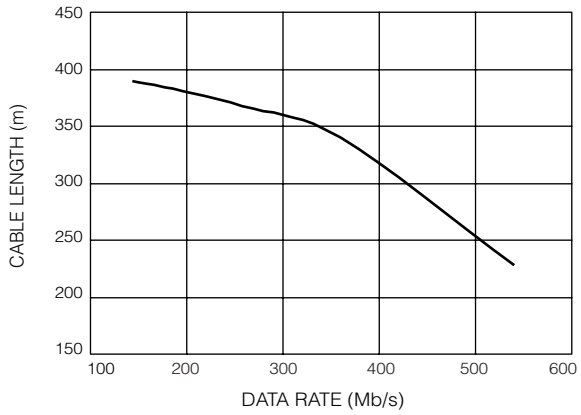


Fig. 7 Typical Error Free Cable Length

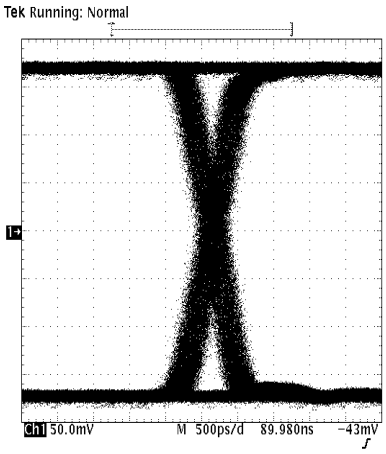


Fig. 8 Intrinsic Jitter (2^{23} - 1 Pattern) 30Mb/s

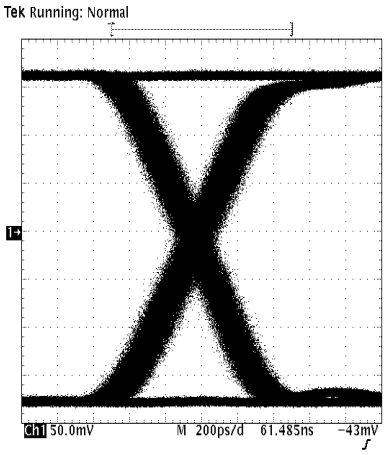


Fig. 9 Intrinsic Jitter (2^{23} - 1 Pattern) 143Mb/s

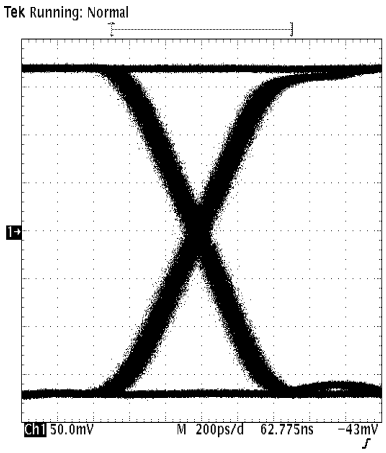


Fig. 10 Intrinsic Jitter (2^{23} - 1 Pattern) 270Mb/s

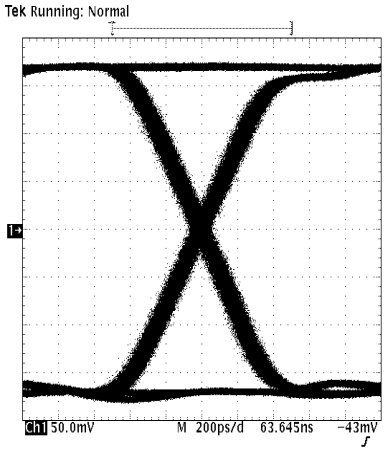
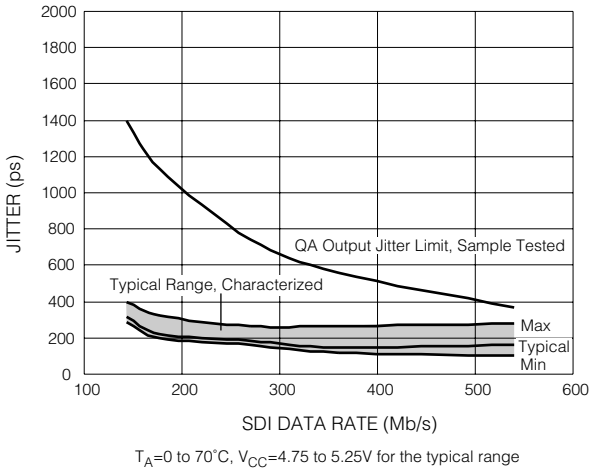
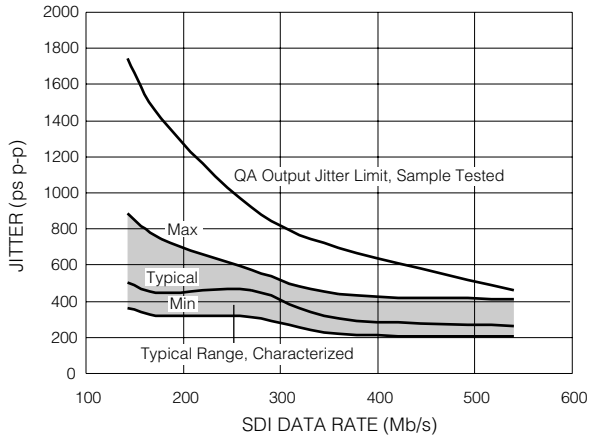


Fig. 11 Intrinsic Jitter (2^{23} - 1 Pattern) 540Mb/s



T_A=0 to 70˚C, V_{CC}=4.75 to 5.25V for the typical range

Fig. 12 Intrinsic Jitter - Pseudorandom (2^{23} - 1)



T_A = 0 to 70˚C, V_{CC} = 4.75 to 5.25V for the typical range

Fig. 13 Intrinsic Jitter - Pathological SDI Checkfield

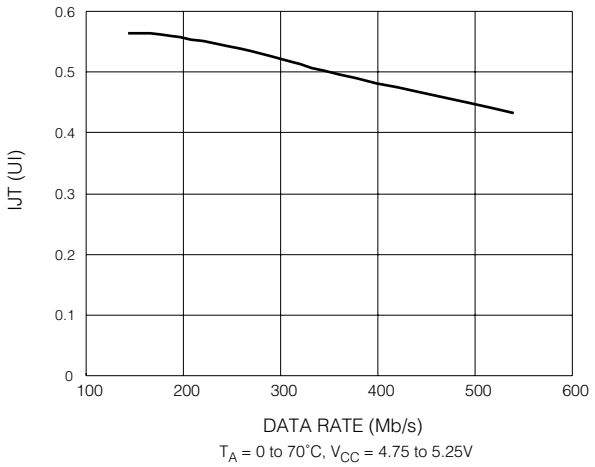


Fig. 14 Typical Input Jitter Tolerance (Characterized)

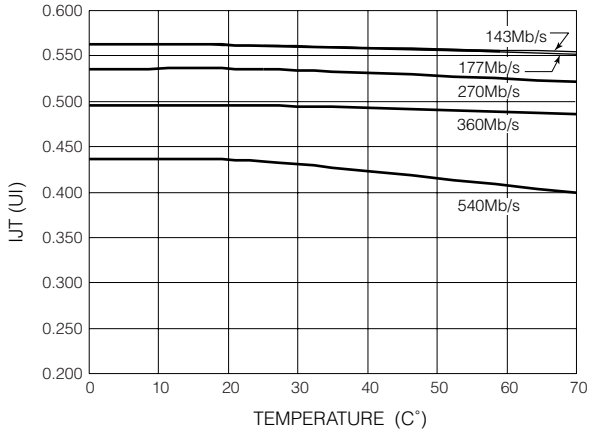


Fig. 15 Typical IJT vs. Temperature (V_{CC} = 5.0V) (Characterized)

DETAILED DESCRIPTION

The GS9025A Serial Digital Receiver is a bipolar integrated circuit containing a built-in cable equalizer and reclocker.

Serial digital signals are applied to either the analog SDI/$\overline{\text{SDI}}$ or digital DDI/$\overline{\text{DDI}}$ inputs. Signals applied to the SDI/$\overline{\text{SDI}}$ inputs are equalized and then passed to a multiplexer. Signals applied to the DDI/$\overline{\text{DDI}}$ inputs bypass the equalizer and go directly to the multiplexer. The analog/digital select pin (A/$\overline{\text{D}}$) determines which signal is then passed to the reclocker.

Packaged in a 44 pin MQFP, the receiver operates from a single 5V supply to data rates of 540Mb/s. Typical power consumption is 575mW.

1. CABLE EQUALIZER

The automatic cable equalizer is designed to equalize serial digital data signals from 143Mb/s to 540Mb/s.

The serial data signal is connected to the input pins (SDI/$\overline{\text{SDI}}$) either differentially or single-ended. The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length. The gain stage provides up to 40dB of gain at 200MHz which typically results in equalization of greater than 350m at 270Mb/s of Belden 8281 cable.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by an external differential AGC filter capacitor (AGC+/AGC-) providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter.

The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its corrective level irrespective of shifts due to AC coupling.

1-1. Signal Strength Indication/carrier Detect

The GS9025A incorporates an analog signal strength indicator/carrier detect (SSI/$\overline{\text{CD}}$) output indicating both the presence of a carrier and the amount of equalization applied to the signal. The voltage output of this pin versus cable length (signal strength) is shown in Figure 2 and Figure 16.

With 0m of cable (800mV input signal levels), the SSI/$\overline{\text{CD}}$ output voltage is approximately 4.5V. As the cable length increases, the SSI/$\overline{\text{CD}}$ voltage decreases linearly providing accurate correlation between the SSI/$\overline{\text{CD}}$ voltage and cable length.

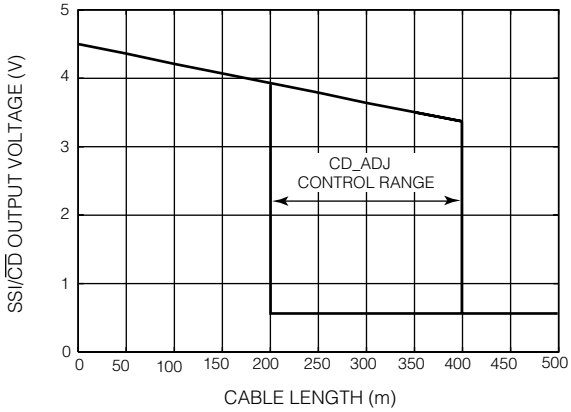


Fig. 16 SSI/$\overline{\text{CD}}$ Voltage vs. Cable Length

When the signal strength decreases to the level set at the "Carrier Detect Threshold Adjust" pin, the SSI/$\overline{\text{CD}}$ voltage goes to a logic "0" state (0.8 V) and can be used to drive

other TTL/CMOS compatible logic inputs. In addition, when loss of carrier is detected, the SDO/$\overline{\text{SDO}}$ outputs are muted (set to a known static state).

1-2. Carrier Detect Threshold Adjust

This feature has been designed for use in applications such as routers where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem since the signal to noise ratio on the circuit board could be significantly less than the default signal detection level set by the on chip reference. To alleviate this problem, the GS9025A provides a user adjustable threshold to meet the unique conditions that exist in each user's application. Override and internal default settings have also been provided to give the user total flexibility.

The threshold level at which loss of carrier is detected is adjustable via external resistors at the CD_ADJ pin. The control voltage at the CD_ADJ pin is set by a simple resistor divider circuit (*see Typical Application Circuit*). The threshold level is adjustable from 200m to 350m. By default (no external resistors), the threshold is typically 320m. In noisy environments, it is not recommended to leave this pin floating. Connecting this pin to V_{EE} disables the SDO/$\overline{\text{SDO}}$ muting function and allows for maximum possible cable length equalization.

1-3. Output Eye Monitor Test

The GS9025A also provides an 'Output Eye Monitor Test' (OEM_TEST) which allows the verification of signal integrity after equalization, prior to reslicing. The OEM_TEST pin is an open collector current output that requires an external 50Ω pullup resistor. When the pullup resistor is not used, the OEM_TEST block is disabled and the internal OEM_TEST circuit is powered down. The OEM_TEST provides a 100mVp-p signal when driving a 50Ω oscilloscope input. Due to additional power consumed by this diagnostic circuit, it is not recommended for continuous operation.

2. RECLOCKER

The reclocker receives a differential serial data stream from the internal multiplexer. It locks an internal clock to the incoming data. It outputs the differential PECL retimed data signal on SDO/$\overline{\text{SDO}}$. It outputs the recovered clock on SCO/$\overline{\text{SCO}}$. The timing between the output and clock signals is shown in Figure 17.

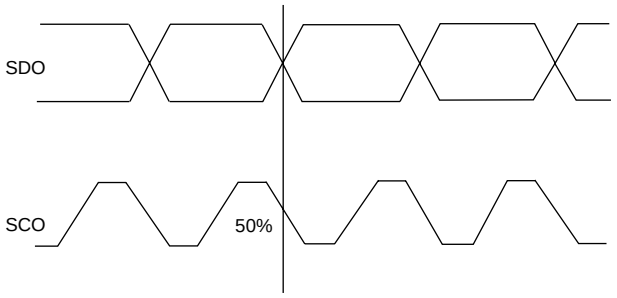


Fig. 17 Output and Clock Signal Timing

The reclocker contains four main functional blocks: the Phase Locked Loop, Auto/Manual Data Rate Select, Frequency Acquisition, and Logic Circuit.

2-1. Phase Locked Loop (PLL)

The Phase Locked Loop locks the internal PLL clock to the incoming data rate. A simplified block diagram of the PLL is shown below. The main components are the VCO, the phase detector, the charge pump, and the loop filter.

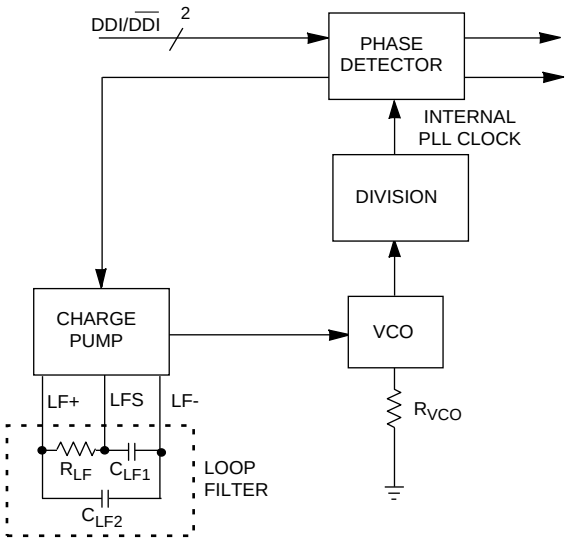


Fig. 18 Simplified Block Diagram of the PLL

2-2. VCO

The VCO is a differential low phase noise, factory trimmed design that provides increased immunity to PCB noise and precise control of the VCO centre frequency. The VCO operates between 30 and 540Mb/s and has a pull range of ±15% about the centre frequency. A single low impedance external resistor, R_{VCO}, sets the VCO centre frequency (*see Figure 19*). The low impedance R_{VCO} minimizes thermal noise and reduces the PLL's sensitivity to PCB noise.

For a given R_{VCO} value, the VCO can oscillate at one of two frequencies. When SMPTE = SS0 = logic 1, the VCO centre frequency corresponds to the f_L curve. For all other SMPTE/SS0 combinations, the VCO centre frequency corresponds to the f_H curve (f_H is approximately 1.5 x f_L).

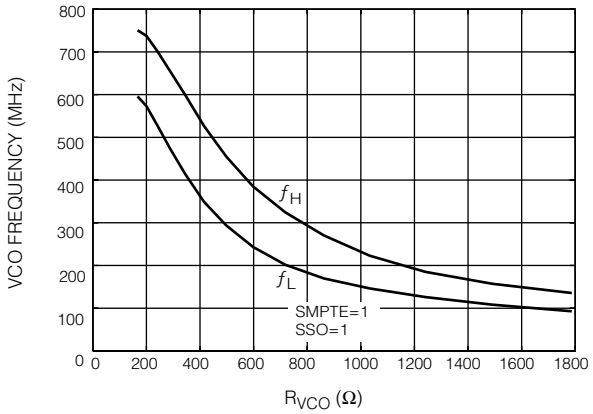


Fig. 19 R_{VCO} vs. VCO Centre Frequency

The recommended R_{VCO} value for auto rate SMPTE 259M applications is 365Ω.

The VCO and an internal divider generate the PLL clock. Divider moduli of 1, 2, and 4 allow the PLL to lock to data rates from 143Mb/s to 540Mb/s. The divider modulus is set by the AUTO/$\overline{\text{MAN}}$, SMPTE, and SS[2:0] pins *(for further details, see section 4, Auto/Manual Data Rate Select)*. In addition, a manually selectable modulus 8 divider allows operation at data rates as low as 30Mb/s.

When the input data stream is removed for an excessive period of time *(see AC electrical characteristics table),* the VCO frequency can drift from the previously locked frequency to the limits shown in Table1.

TABLE 1: Frequency Drift Range (when PLL loses lock)

LOSES LOCK FROM	MIN (%)	MAX(%)
143Mb/s lock	-21	21
177Mb/s lock	-12	26
270Mb/s lock	-13	28
360 Mb/s lock	-13	24
540 Mb/s lock	-13	28

2-3. Phase Detector

The phase detector compares the phase of the PLL clock with the phase of the incoming data signal and generates error correcting timing pulses. The phase detector design provides a linear transfer function which maximizes the input jitter tolerance of the PLL.

2-4. Charge Pump

The charge pump takes the phase detector output timing pulses and creates a charge packet that is proportional to the system phase error. A unique differential charge pump design insures that the output phase does not drift when data transitions are sparse. This makes the GS9025A ideal for SMPTE 259M applications where pathological signals have data transition densities of 0.05.

2-5. Loop Filter

The loop filter integrates the charge pump packets and produces a VCO control voltage. The loop filter is comprised of three external components which are connected to pins LF+, LFS, and LF-. The loop filter design is fully differential giving the GS9025A increased immunity to PCB board noise.

The loop filter components are critical in determining the loop bandwidth and damping of the PLL. Choosing these component values is discussed in detail in the PLL DESIGN GUIDELINES section. Recommended values for SMPTE259M applications are shown in the Typical Application Circuit.

3. FREQUENCY ACQUISITION

The core PLL is able to lock if the incoming data rate and the PLL clock frequency are within the PLL capture range (which is slightly larger than the loop bandwidth). To assist the PLL to lock to data rates outside of the capture range, the GS9025A uses a frequency acquisition circuit.

The frequency acquisition circuit sweeps the VCO control voltage so that the VCO frequency changes from -10% to +10% of the centre frequency. Figure 20 shows a typical sweep waveform.

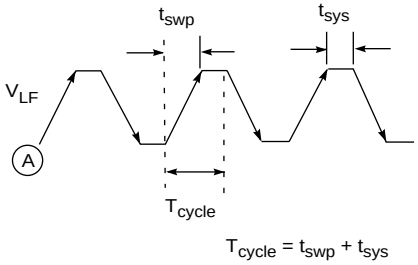


Fig. 20 Typical Sweep Waveform

The VCO frequency starts at point A and sweeps up attempting to lock. If lock is not established during the up sweep, the VCO is then swept down. The system is designed such that the probability of locking within one cycle period is greater than 0.999. If the system does not lock within one cycle period, it will attempt to lock in the subsequent cycle. In manual mode, the divider modulus is fixed for all cycles. In auto mode, each subsequent cycle is based on a different divider moduli as determined by the internal 3-bit counter.

The average sweep time, t_{swp}, is determined by the loop filter component, C_{LF1}, and the charge pump current, I_{CP}:

$$t_{SWP} = \frac{4C_{LF1}}{3I_{CP}}$$

The nominal sweep time is approximately 121µs when C_{LF1} = 15nF and I_{CP} = 165µA (R_{VCO} = 365Ω).

An internal system clock determines t_{sys} *(see section 3-1, Logic Circuit)*.

3-1. Logic Circuit

The GS9025A is controlled by a finite state logic circuit which is clocked by an asynchronous system clock. That is, the system clock is completely independent of the incoming data rate. The system clock runs at low frequencies, relative to the incoming data rate, and thus reduces interference to the PLL.The period of the system clock is set by the COSC capacitor and is:

$$t_{sys} = 9.6 \times 10^4 \times C_{OSC}[\text{seconds}]$$

The recommended value for t_{sys} is 450µs (C_{OSC} = 4.7nF)

4. AUTO/MANUAL DATA RATE SELECT

The GS9025A can operate in either auto or manual data rate select mode. The mode of operation is selected by a single input pin (AUTO/$\overline{\text{MAN}}$).

4-1. Auto Mode (AUTO/$\overline{\text{MAN}}$ = 1)

In auto mode, the GS9025A uses a 3-bit counter to automatically cycle through five (SMPTE=1) or three (SMPTE=0) different divider moduli as it attempts to acquire lock. In this mode, the SS[2:0] pins are outputs and indicate the current value of the divider moduli according Table 2.

NOTE: For SMPTE = 0 and divider moduli of 2 and 4, the PLL can correctly lock for two values of SS[2:0].

4-2. Manual Mode (AUTO/$\overline{\text{MAN}}$ = 0)

In manual mode, the GS9025A divider moduli is fixed. In this mode, the SS[2:0] pins are inputs and set the divider moduli according to Table 3.

5. LOCKING

The GS9025A indicates lock when three conditions are satisfied:

1. Input data is detected.
2. The incoming data signal and the PLL clock are phase locked.
3. The system is not locked to a harmonic.

TABLE 2.

AUTO/$\overline{\text{MAN}}$ = 1 (AUTO MODE)
f_H, f_L = VCO centre frequency as per Figure 19.

SMPTE	SS[2:0]	DIVIDER MODULI	PLL CLOCK
1	000	4	$f_H/4$
1	001	2	$f_L/2$
1	010	2	$f_H/2$
1	011	1	f_L
1	100	1	f_H
1	101	-	-
1	110	-	-
1	111	-	-
0	000	4	$f_H/4$
0	001	4	$f_H/4$
0	010	2	$f_H/2$
0	011	2	$f_H/2$
0	100	1	f_H
0	101	-	-
0	110	-	-
0	111	-	-

TABLE 3.

AUTO/$\overline{\text{MAN}}$ = 1 (MANUAL MODE)
f_H, f_L = VCO centre frequency as per Figure 19.

SMPTE	SS[2:0]	DIVIDER MODULI	PLL CLOCK
1	000	4	$f_H/4$
1	001	2	$f_L/2$
1	010	2	$f_H/2$
1	011	1	f_L
1	100	1	f_H
1	101	8	$f_L/8$
1	110	8	$f_H/8$
1	111	-	-
0	000	4	$f_H/4$
0	001	4	$f_H/4$
0	010	2	$f_H/2$
0	011	2	$f_H/2$
0	100	1	f_H
0	101	1	f_H
0	110	8	$f_H/8$
0	111	-	-

The GS9025A defines the presence of input data when at least one data transition occurs every 1µs.

The GS9025A assumes that it is NOT locked to a harmonic if the pattern '101' or '010' (in the reclocked data stream) occurs at least once every $t_{sys}/3$ seconds. Using the recommended component values, this corresponds to approximately 150µs. In a harmonically locked system, all bit cells are double clocked and the above patterns become '110011' and '001100', respectively.

5-1. Lock Time

The lock time of the GS9025A depends on whether the input data is switching synchronously or asynchronously. Synchronous switching refers to the case where the input data is changed from one source to another source which is at the same data rate (but different phase). Asynchronous switching refers to the case where the input data is changed from one source to another source which is at a different data rate.

When input data to the GS9025A is removed, the GS9025A latches the current state of the counter (divider modulus). Therefore, when data is reapplied, the GS9025A begins the lock procedure at the previous locked data rate. As a result, in synchronous switching applications, the GS9025A locks very quickly. The nominal lock time depends on the switching time and is summarized in the Table 4.

TABLE 4.

SWITCHING TIME	LOCK TIME
<0.5µs	10µs
0.5µs - 10ms	$2t_{sys}$
>10ms	$2T_{cycle} + 2t_{sys}$

In asynchronous switching applications, including power up, the lock time is determined by the frequency acquisition circuit *(see section 3, Frequency Acquisition Circuit)*.

To acquire lock in manual mode, the frequency acquisition circuit may have to sweep over an entire cycle depending on initial conditions. Maximum lock time is $2T_{cycle} + 2t_{sys}$.

To acquire lock in auto tune mode, the frequency acquisition circuit may have to cycle through 5 possible counter states depending on initial conditions. Maximum lock time is $6T_{cycle} + 2t_{sys}$.

The nominal value of T_{cycle} for the GS9025A operating in a typical SMPTE 259M application is approximately 1.3ms.

The GS9025A has a dedicated LOCK output (pin 39) indicating when the device is locked. It should be noted that in synchronous switching applications where the switching time is less than 0.5µs, the LOCK output will NOT be de-asserted and the data outputs will NOT be muted.

6. OUTPUT DATA MUTING

The GS9025A internally mutes the SDO and $\overline{SDO}$ outputs when the device is not locked. When muted, SDO/$\overline{SDO}$ are latched providing a logic state to the subsequent circuit and avoiding a condition where noise could be amplified and appear as data.

The output data muting timing is shown in Figure 21.

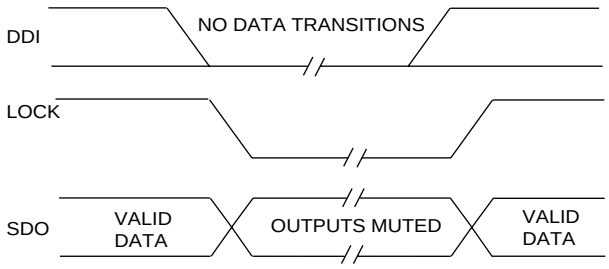


Fig. 21 Output Data Muting Timing

7. CLOCK ENABLE

When CLK_EN is high, the GS9025A SCO/$\overline{SCO}$ outputs are enabled. When CLK_EN is low, the SCO/$\overline{SCO}$ outputs are tri-stated and float to V_{CC}. Disabling the clock outputs results in a power savings of 10%. It is recommended that the CLK_EN input be hard wired to the desired state. For applications which do not require the clock output, connect CLK_EN to Ground and connect the SCO/$\overline{SCO}$ outputs to V_{CC}.

8. STRESSFULL DATA PATTERNS

All PLL's are susceptible to stressful data patterns which can introduce bit errors in the data stream. PLL's are most sensitive to patterns which have long run lengths of 0's or 1's (low data transition densities for a long period of time). The GS9025A is designed to operate with low data transition densities such as the SMPTE 259M pathological signal (data transition density = 0.05).

9. PLL DESIGN GUIDELINES

The reclocking performance of the GS9025A is primarily determined by the PLL. Thus, it is important that the system designer is familiar with the basic PLL design equations.

A model of the GS9025A PLL is shown in Figure 22. The main components are the phase detector, the VCO, and the external loop filter components.

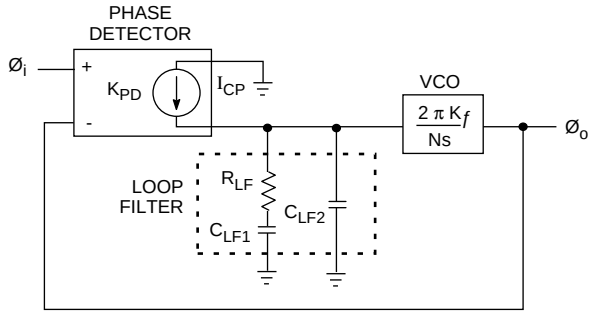


Fig. 22 Model of the GS9025A

9-1. Transfer Function

The transfer function of the PLL is defined as $Ø_o/Ø_i$ and can be approximated as:

$$\frac{Ø_o}{Ø_i} = \frac{sC_{LF1}R_{LF} + 1}{\left[s\left(C_{LF1}R_{LF} - \frac{L}{R_{LF}}\right) + 1\right]} \frac{1}{\left[s^2C_{LF2}L + s\frac{L}{R_{LF}} + 1\right]}$$

Equation 1

where $L = \frac{N}{DI_{CP}K_f}$ and

N is the divider modulus

D is the data density (=0.5 for NRZ data)

I_{CP} is the charge pump current in amps

K_f is the VCO gain in Hz/V

This response has 1 zero (w_Z) and three poles (w_{P1},w_{BW},w_{P2}) where:

$$w_Z = \frac{1}{C_{LF1}R_{LF}}$$

$$w_{P1} = \frac{1}{C_{LF1}R_{LF} - \frac{L}{R_{LF}}}$$

$$w_{BW} = \frac{R_{LF}}{L}$$

$$w_{P2} = \frac{1}{C_{LF2}R_{LF}}$$

The bode plot for this transfer function is plotted in Figure 23.

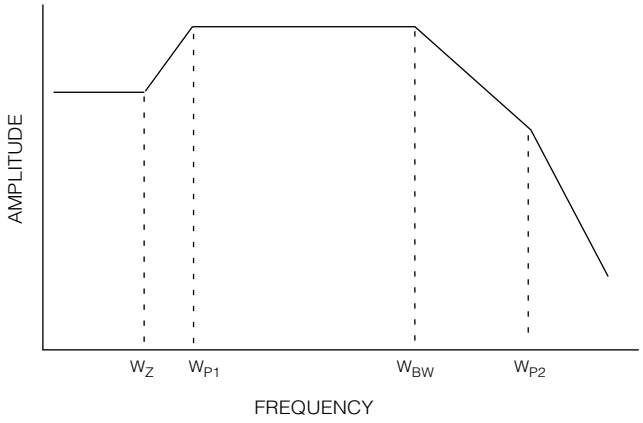


Fig. 23 Transfer Function Bode Plot

The 3dB bandwidth of the transfer function is approximately:

$$w_{3dB} = \frac{w_{BW}}{\sqrt{1 - 2\frac{w_{BW}}{w_{P2}} + \frac{(w_{BW}/w_{P2})^2}{1 - 2\frac{w_{BW}}{w_{P2}}}}} \approx \frac{w_{BW}}{0.78}$$

9-2. Transfer Function Peaking

There are two causes of peaking in the PLL transfer function given by Equation 1.

The first is quadratic:

$$s^2C_{LF2}L + s\frac{L}{R_{LF}} + 1$$

which has:

$$w_o = \frac{1}{\sqrt{C_{LF2}L}} \quad \text{and} \quad Q = R_{LF}\sqrt{\frac{R_{LF2}}{L}}$$

This response is critically damped for Q = 0.5.

Thus, to avoid peaking:

$$R_{LF}\sqrt{\frac{C_{LF2}}{L}} < \frac{1}{2} \quad \text{or} \quad \frac{1}{R_{LF2}C_{LF2}} \frac{L}{R_{LF}} > 4$$

Therefore,

$$w_{P2} > 4\, w_{BW}$$

To reduce the high frequency content on the loop filter, keep w_{P2} as low as possible.

The second is the zero-pole combination:

$$\frac{sC_{LF1}R_{LF} + 1}{s\left(C_{LF1}R_{LF} - \frac{1}{R_{LF}}\right) + 1} = \frac{\frac{s}{w_Z} + 1}{\frac{s}{w_{P1}} + 1}$$

This causes lift in the transfer function given by:

$$20\ LOG\frac{w_{P1}}{w_Z} = 20\ LOG\frac{1}{1-\frac{w_Z}{w_{BW}}}$$

To keep peaking to less than 0.05dB:

$$w_Z < 0.0057 w_{BW}$$

9.3 Selection of Loop Filter Components

Based on the above analysis, the loop filter components should be selected for a given PLL bandwidth, f_{3dB}, as follows:

1. Calculate

$$L = \frac{2N}{I_{CP}K_f}$$

where:

I_{CP} is the charge pump current and is a function of the R_{VCO} resistor and is obtained from Figure 24.

K_f = 90MHz/V for VCO frequencies corresponding to the f_L curve.

K_f = 140MHz/V for VCO frequencies corresponding to the f_H curve.

N is the divider modulus

(f_L, f_H and N can be obtained from Table 2 or Table 3)

2. Choose $R_{LF} = 2(3.14)f_{3dB}(0.78)L$
3. Choose $C_{LF1} = 174L/(R_{LF})^2$
4. Choose $C_{LF2} = L/4(R_{LF})^2$

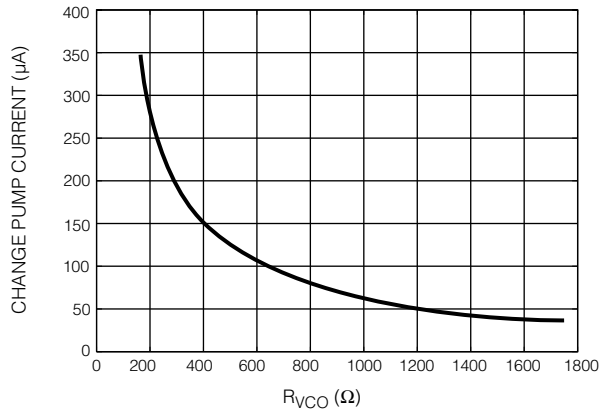
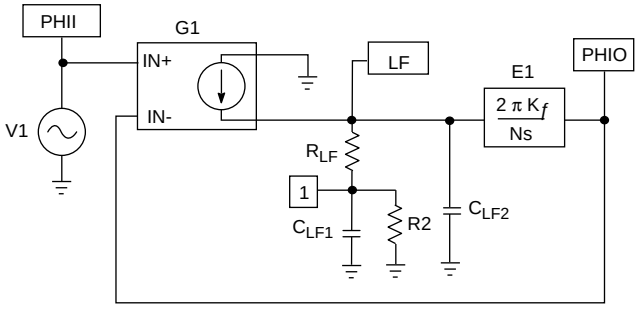


Fig. 24 R_{VCO} vs. Charge Pump Current

9-4. SPICE Simulations

More detailed analysis of the GS9025A PLL can be done using SPICE. A SPICE model of the PLL is shown below:



NOTE: PHII, PHIO, LF, and 1 are node names in the SPICE netlist.

Fig. 25 SPICE Model of the PLL

The model consists of a voltage controlled current source (G1), the loop filter components (R_{LF}, C_{LF1}, and C_{LF2}), a voltage controlled voltage source (E1), and a voltage source (V1). R2 is necessary to create a DC path to ground for Node 1.

V1 is used to generate the input phase waveform. G1 compares the input and output phase waveforms and generates the charge pump current, I_{CP}. The loop filter components integrate the charge pump current to establish the loop filter voltage. E1 creates the output phase waveform (PHIO) by multiplying the loop filter voltage by the value of the Laplace transform ($2\pi K_f/Ns$).

The net list for the model is given below. The .PARAM statements are used to set values for I_{CP}, K_f, N, and D. I_{CP} is determined by the R_{VCO} resistor and is obtained from Figure 24.

```
SPICE NETLIST * GS9025A PLL Model
.PARAM ICP = 165E-6 KF= 90E+6
.PARAM N = 1 D = 0.5
.PARAM PI = 3.14
.IC V(Phio) = 0
.ac dec 30 1k 10meg
RLF 1 LF 1000
CLF1 1 0 15n
CLF2 0 LF 15p
E_LAPLACE1 Phio 0 LAPLACE {V(LF)} {(2*PI*KF)/(N*s)}
G1 0 LF VALUE{D * ICP/(2*pi)*V(Phii, Phio)}
V1 2 0 DC 0V AC 1V
R2 0 1 1g
.END
```

10. I/O DESCRIPTION

10-1. High Speed Analog Inputs (SDI/$\overline{\text{SDI}}$)

SDI/$\overline{\text{SDI}}$ are high impedance inputs which accept differential or single-ended input drive.

Figure 26 shows the recommended interface when a single-ended serial digital signal is used.

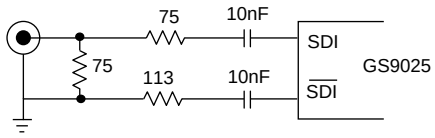


Fig. 26

10-2. High Speed Digital Inputs (DDI/$\overline{\text{DDI}}$)

DDI/$\overline{\text{DDI}}$ are high impedance inputs which accept differential or single-ended input drive. Two conditions must be observed when interfacing to these inputs:

1. Input signal amplitudes are between 200 and 2000 mV
2. The common mode input voltage range is as specified in the DC Characteristics table.

Commonly used interface examples are shown in Figures 27 to 29.

Figure 27 illustrates the simplest interface to the GS9025A digital inputs. In this example, the driving device generates the PECL level signals (800mV amplitudes) having a common mode input range between 0.4 and 4.6V. This scheme is recommended when the trace lengths are less than 1in. The value of the resistors depends on the output driver circuitry.

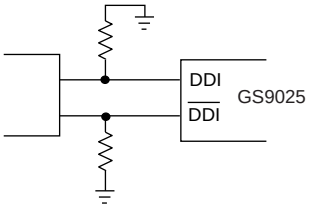


Fig. 27

When trace lengths become greater than 1in, controlled impedance traces should be used. The recommended interface is shown in Figure 29. In this case, a parallel resistor (R_{LOAD}) is placed near the GS9025A inputs to terminate the controlled impedance trace. The value of R_{LOAD} should be twice the value of the characteristic impedance of the trace. In addition, place series resistors (R_{SOURCE}) near the driving chip to serve as source terminations. They should be equal to the value of the trace impedance. Assuming 800mV output swings at the driver, R_{LOAD} = 100Ω, R_{SOURCE} = 50Ω and Z_O = 50Ω.

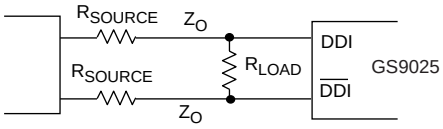


Fig. 28

Figure 29 shows the recommended interface when the GS9025A digital inputs are driven single-endedly. In this case, the input must be AC-coupled and a matching resistor (Z_o) must be used.

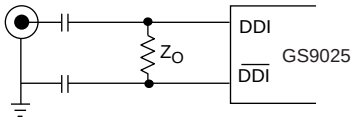


Fig. 29

When the DDI and the $\overline{\text{DDI}}$ inputs are not used, saturate one input of the differential amplifier for improved noise immunity. To saturate, connect either pins 44 and 1 or pins 2 and 3 to V_{CC}. Leave the other pair floating.

10-3. High Speed Outputs (SDO/$\overline{\text{SDO}}$ and SCO/$\overline{\text{SCO}}$)

SDO/$\overline{\text{SDO}}$ and SCO/$\overline{\text{SCO}}$ are current mode outputs that require external pullups (*see Figure 30*). The output signal swings are 800mV when 75Ω resistors are used. To shift the signal levels down by approximately 0.7 volts, place a diode between V_{CC} and the pullups. When the output traces are longer than 1in, use controlled impedance traces. Place the pullup resistors at the end of the output traces as they terminate the trace in its characteristic impedance (75Ω).

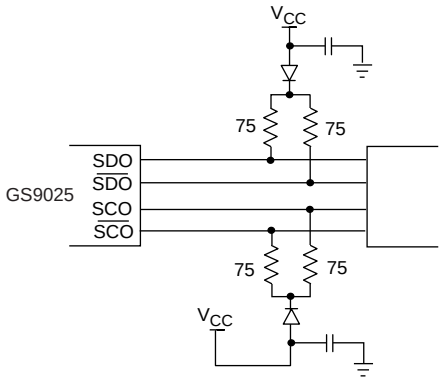
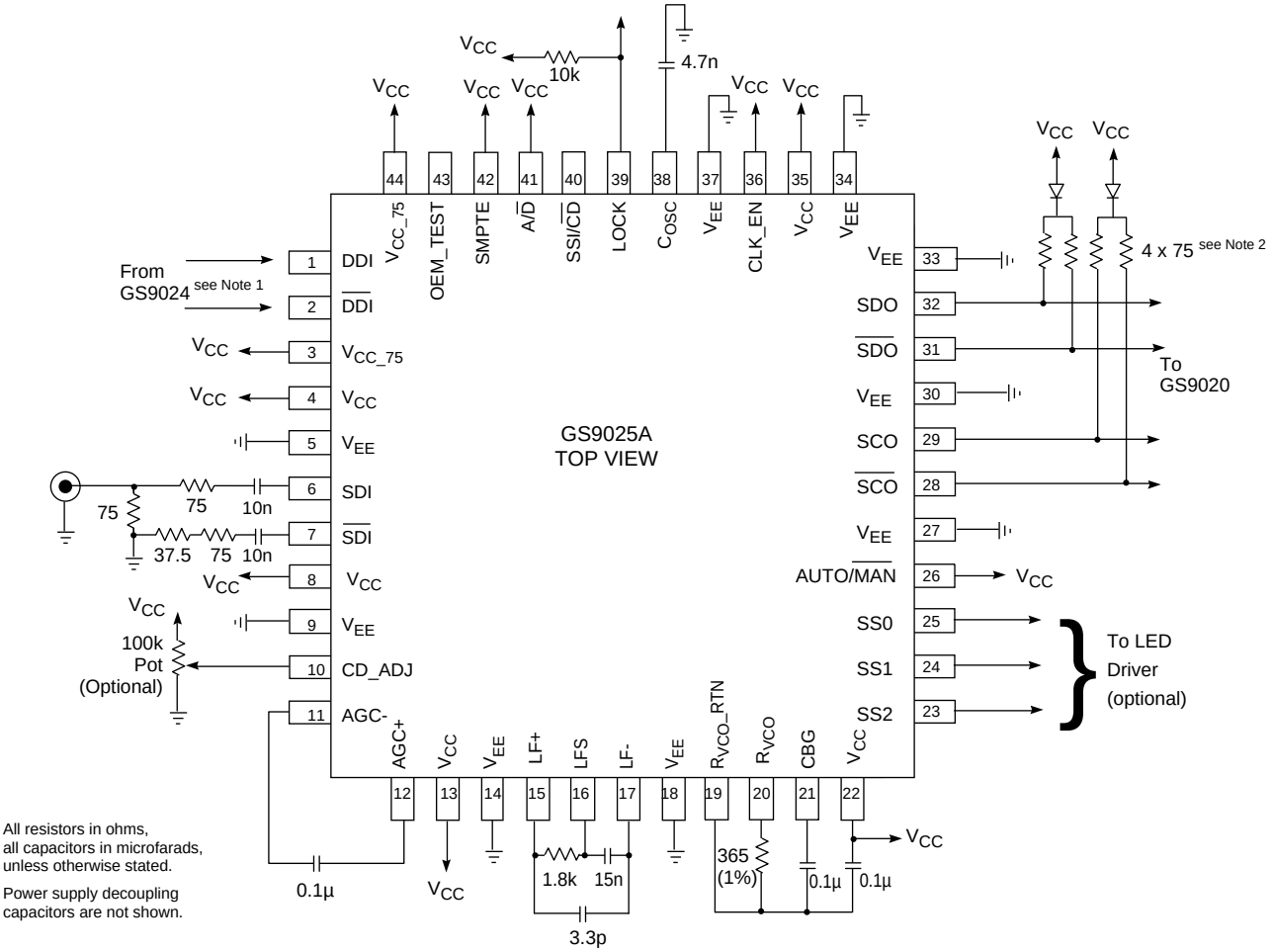


Fig. 30

TYPICAL APPLICATION CIRCUIT

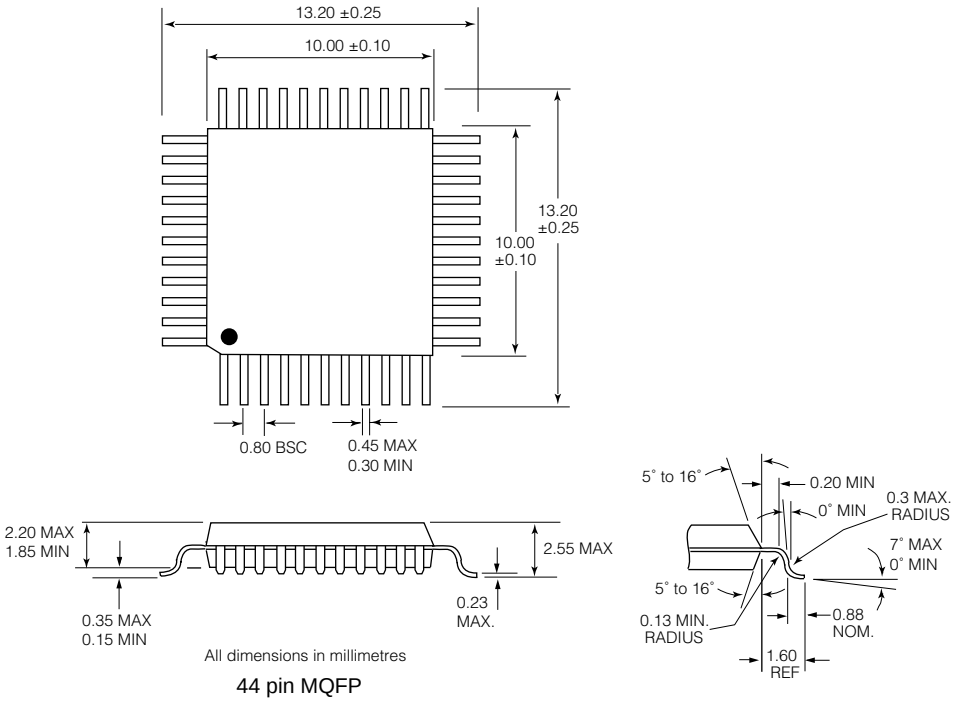

GS9025A
TOP VIEW
From GS9024 see Note 1
To GS9020
4 x 75 see Note 2
To LED Driver (optional)
100k Pot (Optional)
All resistors in ohms, all capacitors in microfarads, unless otherwise stated.
Power supply decoupling capacitors are not shown.

NOTES
1. It is recommended that the DDI/$\overline{\text{DDI}}$ inputs are not driven when the SDI/$\overline{\text{SDI}}$ inputs are being used. This minimizes crosstalk between the DDI/$\overline{\text{DDI}}$ and SDI/$\overline{\text{SDI}}$ inputs and maximizes performance.
2. These resistors are not needed if the internal pull-up resistors on the GS9020 are used.

TABLE 5. R_{VCO} = 365, f_H = 540MHz, f_L = 360MHz

SMPTE	SS[2:0]	DATA RATE (Mb/s)	LOOP BANDWIDTH (MHz)
1	000	143	1.2
1	001	177	1.9
1	010	270	3.0
1	011	360	4.5
1	100	540	6.0

PACKAGE DIMENSIONS



44 pin MQFP

CAUTION

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SENSITIVE DEVICES

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